

TITLE 400G OSFP-RHS SR4 Transceiver	DOC No. RFD-20240112002-003	
	REVISION : 01	AUTHORIZED BY : Andy Yang
	DATE : 2024.08.14	CLASSIFICATION : CONFIDENTIAL

1. PRODUCT FEATURES

- Hot-pluggable OSFP 400G SR4 multimode transceiver
- Compliant with OSFP RHS
- Compliant with CMIS Rev 5.0 and above revision
- 4-channels of 100G-PAM4 electrical and optical modulation
- Maximum power consumption 8.5W with 4 channels and 6.5W with 2 channels
- Single MPO-12 APC receptacles
- Up to 30m reach on OM3 and 50m reach on OM4
- Operates as a 200Gb/s NDR200 transceiver with 2-fiber splitter ends
- Case operating temperature 0°C to 70°C



2. PRODUCT DESCRIPTION

2.1 PRODUCT NAME

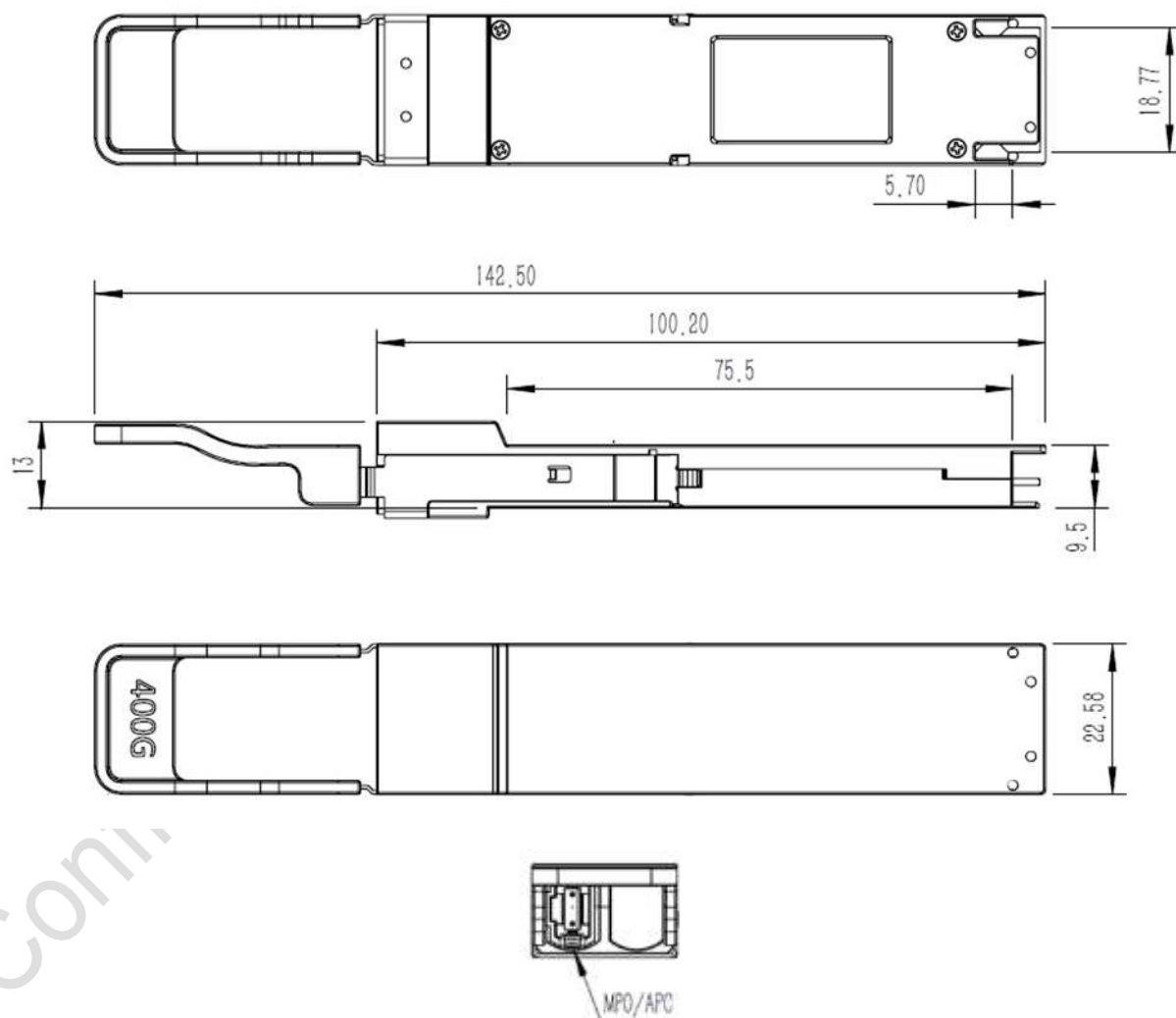
400G OSFP-RHS SR4 Transceiver

JPC P/N	Data Rate	Wavelength(nm)	Optical Power	Sensitivity	Connector	Temp.
P69**4GRCA01-1	400G	850nm	-4.6 ~ 4 dBm	-4.4 dBm	MPO-12	C

Notes : ** Indicates the customer code.

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2.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING



Unit is millimeter. All dimensions are mm unless otherwise specified.

3. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- 400G Ethernet
- Data Center Interconnect
- Enterprise Networking

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4. Product specifications

4.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_s	-40	85	°C	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Control Input Voltage	V_I	-0.3	$V_{CC}+0.5$	V	

4.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	$I_{CC\ IP}$	-	-	3600	mA	
Sustained peak current at hot plug	$I_{CC\ SP}$	-	-	3000	mA	
Maximum Power Dissipation(400G)	P_D	-	-	8.5	W	
Maximum Power Dissipation(200G)	P_D	-	-	6.5	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	1.5	W	
Signaling Rate per Lane	SRL	-	53.125	-	GBd	PAM4
Two Wire Serial Interface Clock Rate	-	-100	-	400	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)	-	-	-	66	mV	
Rx Differential Data Output Load	-	-	100	-	Ohm	
Operating Distance (OM3)	-	2	-	30	m	
Operating Distance (OM4)	-	2	-	50	m	

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4.3 Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λ_C	844	850	863	nm	
RMS spectral width	$\Delta\lambda_{rms}$			0.6	nm	
Average Launch Power, each lane	AOP_L	-4.6	-	4.0	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	T_{OMA}	-2.6		3.5	dBm	2
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	4.4	dB	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-30	dBm	
Extinction Ratio, each lane	ER	2.5		-	dB	
$RIN_{21.4OMA}$	RIN	-	-	-132	dB/Hz	
Optical Return Loss Tolerance	ORL		-	12	dB	
Transmitter Reflectance	T_R	-	-	-26	dB	3

Notes

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if max (TECQ, TDECQ) < 1.8dB, OMA_{outer} (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.

4.4 Receiver Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λ_C	842	850	863	nm	
Damage Threshold, average optical power, each lane	AOP_D	5	-	-	dBm	
Average Receive Power, each lane	AOP_R	-6.3	-	4.0	dBm	
Receive Power (OMA_{outer}), each lane	OMA_R	-	-	3.5	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMA_{outer}), each lane	S_{OMA}	-	-	-4.4	dBm	1
Stressed Receiver Sensitivity (OMA_{outer}), each lane	SRS	-	-	-1.8	dBm	2
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4	SECQ		4.4		dB	
OMA_{outer} of each aggressor lane	OMA_{outer}		3.5		dBm	

Notes:

1. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with TDECQ ≤ 1.8 dB
2. Measured with conformance test signal at TP3 for the BER = 2.4x10⁻⁴

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4.5 Electrical Specification High Speed Signal

Receiver (Module Output, TP4)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
AC common-mode output Voltage (RMS)		-	-	25	mV	
Differential output Voltage (Long mode)		-	-	845	mV	
Differential output Voltage (Short mode)		-	-	600	mV	
Near-end Eye height, differential		70	-	-	mV	
Far-end Eye height, differential		30	-	-	mV	
Far end pre-cursor ratio		-4.5	-	2.5	%	
Differential Termination Mismatch		-	-	10	%	
Transition Time (min, 20% to 80%)		9.5	-	-	ps	
DC common mode Voltage		-350	-	2850	mV	

Transmitter (Module Input, TP1)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential pk-pk input Voltage tolerance		750	-	-	mV	
Differential termination mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common mode Voltage		-350	-	2850	mV	

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4.6 Electrical Specification Low Speed Signal

Parameter	Symbol	Min.	Max.	Unit	Notes
Module output SCL and SDA	V _{OL}	0	0.4	V	
	V _{OH}	V _{CC} -0.5	V _{CC} +0.3	V	
Module Input SCL and SDA	V _{IL}	-0.3	V _{CC} *0.3	V	
	V _{IH}	V _{CC} *0.7	V _{CC} +0.5	V	

5. OSFP Edge Connector and Pinout Description

Top Side (viewed from top)

60	GND	
59	TX1p	
58	TX1n	
57	GND	
56	TX3p	
55	TX3n	
54	GND	
53	TX5p	
52	TX5n	
51	GND	
50	TX7p	
49	TX7n	
48	GND	
47	SDA	
46	VCC	
45	VCC	
44	INT/RSTn	
43	GND	
42	RX8n	
41	RX8p	
40	GND	
39	RX6n	
38	RX6p	
37	GND	
36	RX4n	
35	RX4p	
34	GND	
33	RX2n	
32	RX2p	
31	GND	

----- Module Card Edge -----

Bottom Side (viewed from bottom)

	GND	1
	TX2p	2
	TX2n	3
	GND	4
	TX4p	5
	TX4n	6
	GND	7
	TX6p	8
	TX6n	9
	GND	10
	TX8p	11
	TX8n	12
	GND	13
	SCL	14
	VCC	15
	VCC	16
	LPWn/PRSn	17
	GND	18
	RX7n	19
	RX7p	20
	GND	21
	RX5n	22
	RX5p	23
	GND	24
	RX3n	25
	RX3p	26
	GND	27
	RX1n	28
	RX1p	29
	GND	30

Pin#	Logic	Symbol	Description	Direction	Plug Sequence	Notes
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1		GND	Ground		1	
2	CML-I	TX2p	Transmitter Data Non-Inverted	Input from Host	3	
3	CML-I	TX2n	Transmitter Data Inverted	Input from Host	3	
4		GND	Ground		1	
5	CML-I	TX4p	Transmitter Data Non-Inverted	Input from Host	3	
6	CML-I	TX4n	Transmitter Data Inverted	Input from Host	3	
7		GND	Ground		1	
8	CML-I	TX6p	Transmitter Data Non-Inverted	Input from Host	3	Not used
9	CML-I	TX6n	Transmitter Data Inverted	Input from Host	3	Not used
10		GND	Ground		1	
11	CML-I	TX8p	Transmitter Data Non-Inverted	Input from Host	3	Not used
12	CML-I	TX8n	Transmitter Data Inverted	Input from Host	3	Not used
13		GND	Ground		1	
14	LVC MOS-I/O	SCL	2-wire Serial interface clock	Bi-directional	3	
15		VCC	+3.3V Power	Power from Host	2	
16		VCC	+3.3V Power	Power from Host	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	Bi-directional	3	
18		GND	Ground		1	

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19	CML-O	RX7n	Receiver Data Inverted	Output to Host	3	Not used
20	CML-O	RX7p	Receiver Data Non-Inverted	Output to Host	3	Not used
21		GND	Ground		1	
22	CML-O	RX5n	Receiver Data Inverted	Output to Host	3	Not used
23	CML-O	RX5p	Receiver Data Non-Inverted	Output to Host	3	Not used
24		GND	Ground		1	
25	CML-O	RX3n	Receiver Data Inverted	Output to Host	3	
26	CML-O	RX3p	Receiver Data Non-Inverted	Output to Host	3	
27		GND	Ground		1	
28	CML-O	RX1n	Receiver Data Inverted	Output to Host	3	
29	CML-O	RX1p	Receiver Data Non-Inverted	Output to Host	3	
30		GND	Ground		1	
31		GND	Ground		1	
32	CML-O	RX2p	Receiver Data Non-Inverted	Output to Host	3	
33	CML-O	RX2n	Receiver Data Inverted	Output to Host	3	
34		GND	Ground		1	
35	CML-O	RX4p	Receiver Data Non-Inverted	Output to Host	3	
36	CML-O	RX4n	Receiver Data Inverted	Output to Host	3	

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37		GND	Ground		1	
38	CML-O	RX6p	Receiver Data Non-Inverted	Output to Host	3	Not used
39	CML-O	RX6n	Receiver Data Inverted	Output to Host	3	Not used
40		GND	Ground		1	
41	CML-O	RX8p	Receiver Data Non-Inverted	Output to Host	3	Not used
42	CML-O	RX8n	Receiver Data Inverted	Output to Host	3	Not used
43		GND	Ground		1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	Bi-directional	3	
45		VCC	+3.3V Power	Power from Host	2	
46		VCC	+3.3V Power	Power from Host	2	
47	LVC MOS-I/O	SDA	2-wire Serial interface data	Bi-directional	3	
48		GND	Ground		1	
49	CML-I	TX7n	Transmitter Data Inverted	Input from Host	3	Not used
50	CML-I	TX7p	Transmitter Data Non-Inverted	Input from Host	3	Not used
51		GND	Ground		1	
52	CML-I	TX5n	Transmitter Data Inverted	Input from Host	3	Not used
53	CML-I	TX5p	Transmitter Data Non-Inverted	Input from Host	3	Not used
54		GND	Ground		1	

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55	CML-I	TX3n	Transmitter Data Inverted	Input from Host	3	
56	CML-I	TX3p	Transmitter Data Non-Inverted	Input from Host	3	
57		GND	Ground		1	
58	CML-I	TX1n	Transmitter Data Inverted	Input from Host	3	
59	CML-I	TX1p	Transmitter Data Non-Inverted	Input from Host	3	
60		GND	Ground		1	

6. Modification History

Rev.	Comments	Date	Originator	Approval
01	Initial	2024/08/14	Andy Yang	Mike Sun